CIF:modelling and analysis of heterogeneous models

Part I

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Contents

Part I

- Heterogeneous models in supervisory control system design
- CIF language and tools for
  - simulation, visualization
  - synthesis, verification
  - code generation for co-simulation and real-time control

Part II

- Case: baggage handling control system design
- Demo: CIF tooling for supervisory control synthesis
Traditional control system design multiple backends

Causes of observed errors?

- System Requirements and Design
- Plant Requirements and Design
- Control Requirements and Design

PLC Coder

IEC 61131-3

C Coder

C code

... Coder
In the traditional way of working, the causes of errors are difficult to find:

- Architect and coders speak different languages, leading to misunderstandings
- Informal requirements can be:
  - ambiguous: interpreted different by architect and coders
  - inconsistent
  - erroneous and incomplete
- Coding errors and backend specific coding errors can be present
- On site adaptations not always reflected in code base

This leads to:

- long delays, many design/coding/testing iterations
- high cost
- inflexibility, difficult to make substantial changes
Controller design with code generation

Causes of observed errors?
Controller design with code generation + co-simulation

- Architect
- Control Requirements and Design
- Control System Modeller
- Verification Model
- Control Model
- System Requirements and Design
- Plant Requirements and Design
- Plant Modeller
- Emulation Model
- Emulation
- Co-simulation
- Commissioning
- Plant Realization
- Causes of observed errors?
Examples:

- SCADE suite by Esterel
  - Data flow modeling of controller
  - Simploter tool for modeling of plant

- Matlab / Simulink
  - Stateflow for modeling of discrete-event control
  - Simulink for modeling of predominantly continuous plants
Control system design using CIF

Few remaining errors in commissioning

 Causes of observed errors?

System Requirements and Design

Control Requirements and Design

Plant Requirements and Design

CIF Control Model

Verification

- Uppaal
- mCRL2
- NuSMV protot

generate

Code generation for various targets

- IEC 61131-3
- Siemens PLC
- C

Emulation

- Simulation and visualization

Commissioning

Planta Realization

- Emulation Model

- CIF Plant Model

- Plant Realization

- Controller Realization

Controller Requirements and Design

- IEC 61131-3

- Siemens PLC

- C

Plant Emulation

- Emulation Model

- CIF Plant Model

- Plant Realization

- Controller Realization

Controller Requirements and Design

- IEC 61131-3

- Siemens PLC

- C

System Requirements and Design

- Controller Requirements and Design

- IEC 61131-3

- Siemens PLC

- C

- Emulation Model

- CIF Plant Model

- Plant Realization

- Controller Realization

- IEC 61131-3

- Siemens PLC

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- C
Iterative simulation-based improvement of control requirements and plant models

Control system design

- System Requirements and Design
  - Architect
  - Modeller
- Control Requirements Model
  - Control Model synthesis
- CIF Control Model
  - Simulation and visualization
  - Generate
  - Verification
    - Uppaal
    - mCRL2
    - NuSMV protot
    - IEC 61131-3
    - Siemens PLC
    - C
- Plant Requirements and Design
- CIF Plant Model
  - Generate
  - Plant Realization

Control system synthesis
CIF overview recent status

CIF Eclipse editor
- Integrated syntax/type checker
- Intuitive error reporting and highlighting

CIF simulator
- Interactive SVG visualization
- Interactive trace exploration
- Plot and state visualizer

Supervisory controller synthesis
- Event-based synthesis
- Data-based synthesis

CIF tooling common features
- Open source with free license: MIT
- Easy install for Windows, Linux and Mac
- IDE and command line releases
- Cross-platform ToolDef 2 scripting
- Based on open standards
- Industrial quality coding standards
- Long history of international development

CIF language
- Hybrid automata
- Theoretical foundation: formal semantics
- Global read, local write variables
- Differential algebraic equations
- Invariants
- Shared events: multi-party synchronization
- Channels: point-to-point communication
- Wide range of data-types
- Stochastic distributions
- Parameterized automata and groups
- Imports

CIF website and documentation
- Extensive language tutorial
- All tooling documented in detail
- http://cif.se.wtb.tue.nl

CIF to yEd GraphML transformer
- Graphical automata diagrams
- Graphical model interaction diagrams

Co-simulation
- CIF to Matlab/Simulink S-function

Verification and synthesis
- CIF to Uppaal
- CIF to mCRL2
- CIF to NuSMV prototype
- CIF to Supremica

Real-time code generation
- CIF to IEC 61131-3: PLC Structured Text
- CIF to C
- CIF to Java
Examples browser

Editor with “as you type” syntax checker

Eclipse: cross-platform open source IDE

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CIF screenshot

Plotting

SVG interactive visualization

State visualizer for debugging

Console for textual output

- Editor with "as you type" syntax checker
- Examples browser
- Plotting
- SVG interactive visualization
- State visualizer for debugging
- Console for textual output

Eclipse: cross-platform open source IDE

Examples

- Editor with "as you type" syntax checker
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Eclipse: cross-platform open source IDE
CIF documentation: 200+ webpages

CIF 3

Welcome to the website for CIF 3, the Compositional Interchange Format for hybrid systems. CIF is a automata-based modeling language for the specification of discrete event, timed, and hybrid systems. The CIF 3 tooling supports the entire development process of controllers, including specification, supervisory controller synthesis, simulation-based validation and visualization, verification, real-time testing, code generation, etc.

CIF 3 was created and is currently developed by the Systems Engineering group of the Mechanical Engineering department at the Eindhoven University of Technology (TU/e).

The CIF 3 tooling is free, and is available under the MIT open source license.

Information

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- Download
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Documentation

- Language tutorial
- CIF 3 textual syntax (PDF)
- Event-based supervisory controller
- Tools
- Changelog for version r7363

Supervisory controller synthesis

- Event-based synthesis toolset
- CIF to Supremica transformer
- CIF to SCIM transformer

Simulation, validation, and visualization

- CIF 3 simulator
- CIF 3 to CIF 2 transformer

Verification

- CIF to mCRL2 transformer
- CIF to Supremica transformer

Real-time testing, code generation, and implementation

- CIF 3 PLC code generator

Miscellaneous

- CIF to CIF transformer
- CIF merger
- CIF 3 event disabler
CIF co-simulation

Cosimulation via
S-function
in Matlab / Simulink

Slide:
Uni Dortmund / Christian Sonntag